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Sub-Threshold Leakage Current Reduction Techniques In VLSI Circuits -A Survey

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ABSTRACT
There is an increasing demand for portable devices powered up by battery, this led the manufacturers of semiconductor technology to scale down the feature size which results in reduction in threshold voltage and enables the complex functionality on a single chip. By scaling down the feature size the dynamic power dissipation has no effect but the static power dissipation has become equal or more than that of Dynamic power dissipation. So in recent CMOS technologies static power dissipation i.e. power dissipation due to leakage current has become a challenging area for VLSI chip designers. In order to prolong the battery life and maintain reliability of circuit, leakage current reduction is the primary goal. A basic overview of techniques used for reduction of sub-threshold leakages is discussed in this paper. Based on the surveyed techniques, one would be able to choose required and apt leakage reduction technique.

Keywords **–**feature size, leakage power, subthreshold leakage current

I. INTRODUCTION

In VLSI circuit design power dissipation is regarded as top-priority issue. In the present scenario, one of the challenging problem to a VLSI designer is to find new and effective techniques so as to reduce the overall power dissipation of the circuit without much compromising its performance. Highly desirable aspect of VLSI circuits is the low power consumption of the circuit with high performance as it directly relates to reliability, battery life, heat removal costs and packaging,. To achieve improved performance and functionality of the devices, scaling is being done since decades. Scaling increases power-density. In 65nm and below technologies has higher dynamic current and leakage current density with minimal improvement in speed. Dynamic power consumption of the circuit is reduced as a result of scaling Vdd but its performance is degraded.[1] This performance degradation can be partially compensated by lowering threshold voltage but at the cost of increased leakage power. Therefore, leakage current has become a primary concern for low-power, high-performance digital CMOS circuits and became major contributor to power consumption with the trend technology scaling. In 65 nm and below technologies, leakage accounts for 30-40% of processor power.[2]

Leakage current is because of sub-threshold leakage, gate-oxide tunneling leakage, reverse bias p-n junction leakage, gate induced drain leakage and punch through current.[3]The leakage current is mainly due to the result of reverse biased PN junction leakage and Sub threshold leakage hence other currents can be neglected. When compared to sub-threshold leakage, the reverse bias PN junction leakage can be ignored. Sub threshold leakage current increases exponentially with lowering of threshold voltage. The sub-threshold leakage is due to the current that flows between drain and source of a MOSFET in weak inversion region.[2]

$$I_{sub}= I_{so}\exp(V_{gs}- V_{th}/ V_{th})(1-\exp(-V_{ds}/V_T)) \quad (1)$$

$$I_{so}=\mu_0 C_{ox}W_{eff}/L_{eff}V^2e^{1.8} \quad (2)$$

Where μ0 is the '0' bias electron mobility
n is the subthreshold slope coefficient
Vgs and Vds are the gate-to-source voltage and drain-to-source voltage respectively
VT is the thermal voltage
Vth is the threshold voltage
Cox is the oxide capacitance per unit area
Weff and Leff are the effective channel width and length respectively

To reduce leakage power due to sub-threshold voltage, several techniques have been proposed such as sleepy keeper, sleepy stacking technique, sleepy transistor technique, multi-Vth, dual-Vth, optimal standby input vector selection, LECTOR method, etc.

In the next section of the paper, various techniques for leakage power reduction due to sub-threshold leakage are described.

II. A SURVEY ON LEAKAGE REDUCTION TECHNIQUES

For sub-threshold leakage power reduction the following are the techniques:

1. Sleep Transistor Technique:

In sleep transistor approach, additional sleep transistors are introduced into the network. One sleep PMOS transistor is placed between VDD and pull up network and other sleep NMOS transistor is placed between pull down network and ground. The circuit operates as follows: In standby mode, the power rails are cut off from the circuit as the sleep transistors are turned off. As a result leakage current in the circuit is reduced.[4][5]

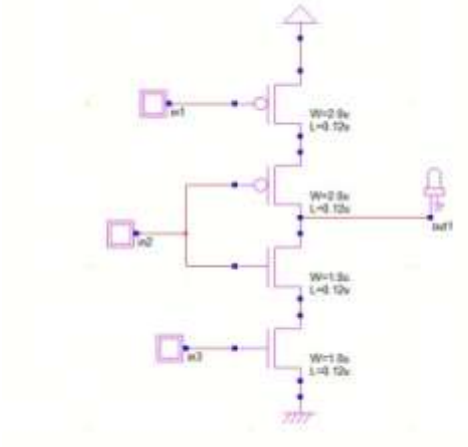

Fig 1 Sleepy Transistor

2. Sleepy Stack Technique:

Other technique to reduce leakage current is by stacking of the transistor. Stacking of the transistor is done by dividing pull up and pull down networks into half size where this doesn't affect W/L ratio of given circuit. Sleepy stack technique is a combination of both sleep transistor approach and stack transistor approach. This technique divides existing transistors circuit into two half length transistors and sleep transistor is added in parallel to the divided circuit. [5]

There are two modes of operation: active mode and sleep mode. During the sleep mode, sleep transistors are turned off. The function of sleep transistor in this circuit is same as in sleep transistor technique. In active mode, sleep transistors are turned on. Each transistor in a conventional circuit is replaced by three transistors in this technique thereby increasing area of the circuit.

The stacked transistor suppresses leakage current while saving state. The sleep transistor and the stacked transistor in each network are made parallel. In this technique, the width of the sleep transistors is reduced. Additional tradeoffs between delay, power and area occur by changing the width of the sleep transistors.[4]

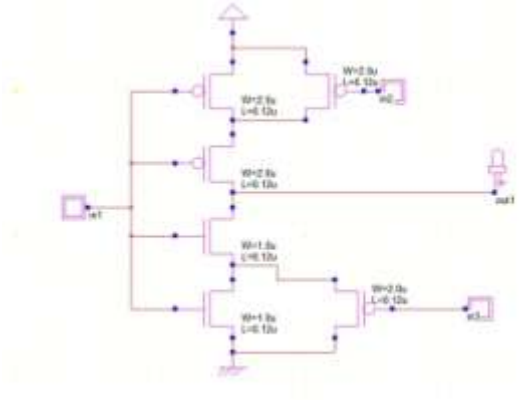

Fig 2 Sleepy Stack Technique

3. Sleepy Keeper:

In Sleepy Keeper additional NMOS is placed in parallel to pull-up sleep transistor which connects VDD to pull-up Network and an additional PMOS is placed in parallel to Pull-down sleep transistor which connects Pull-down Network to the Ground.[9] So the state is saved in sleep mode. Dual Threshold Voltages can also be applied to reduce sub-threshold leakage Current. [4]

In terms of area overhead reduction, sleepy keeper is an excellent alternative to sleepy stack since three transistors in sleepy stack are replaced with one transistor in sleepy keeper. Other advantage of this sleepy keeper technique is that it reduces the sub-threshold leakage current and also retains the present state of the circuit in sleep mode. [6]

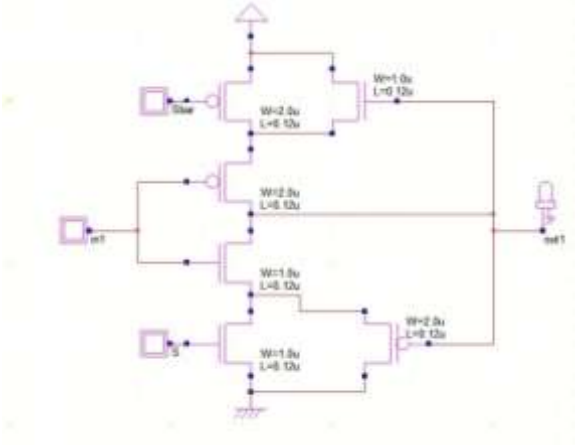

Fig 3 Sleepy Keeper

4. Forced Stacking:

In this technique an additional transistor is introduced for every input of gate in both P and N networks. For every off input two transistors are off instead of one, which induces reverse bias between the transistors resulting in reduction of leakage current. Through this approach huge leakage power

saving is achieved while retaining the logic state. However because of the loading requirements for each input, drive current of gate is reduced. This results in a decreasing the speed of the circuit.[2]

Threshold CMOS:
One of the methods of reducing leakage current is by increasing threshold voltages of transistors.

5. Dual threshold CMOS:

Increasing threshold voltage of transistor is not always possible therefore different paths are set for high threshold and low threshold devices . High-threshold voltage devices are used on non-critical paths in order to reduce the leakage power while using low-threshold devices on critical paths for maintaining circuit performance. This technique is called as Dual threshold CMOS (DTMOS) technique and uses an algorithm in search of gates where high threshold voltage devices can be used.[7] In DTMOS, the body and the gate of each transistor are tied together such that when the device is off, the leakage is low. Current is high if the device is on.

This technique is good for leakage power reduction during standby as well as active modes without delay and area overhead.[3]

6. Variable threshold CMOS:

Other method for modifying threshold voltage of a transistor is by variable threshold CMOS technique (VTCMOS).In this technique during standby mode, threshold voltage (Vth) is raised by making substrate voltage either higher than supply voltage (for PMOS) or lower than ground (for NMOS). During active mode, a slight forward substrate bias can be used to increase circuit speed. In this technique, an additional power supply is required by the circuit which may be a drawback for commercial designs.[8] But extra circuitry is not needed in case of data retention.

7. Multiple threshold CMOS:

MTCMOS is a technique to design CMOS circuit using low, normal and high voltage transistors. Using this technique, selective scaling of threshold voltage is done along with supply voltage so as to increase the circuit speed without increasing the sub-threshold leakage currents. Therefore, this technique provides high speed as well as low power operation using both high threshold and low threshold transistors.[9]The propagation delay time in the critical path can be reduced by low threshold voltage transistors and the power consumption in the shortest path is reduced by high threshold voltage transistors.

There are two modes of operation:active mode and sleep mode. Sleep transistors in MTCMOS circuits are controlled by a “sleep” signal that is used for the active/standby mode control. A virtual supply rail or virtual ground rail are created by connecting sleep transistors between logic circuit and power or ground. Usually in standby state there is much leakage current and this leakage current can be reduced by using high threshold transistors (sleep transistors). Both PMOS and NMOS transistors can be used as sleep transistors but by employing NMOS transistor as sleep transistor, the performance of the circuit is enhanced.[8][10]

Standby leakage power is reduced using this technique but the area and delay of the circuit are increased because of the insertion of large MOSFETs.[11] To reduce the area, one transistor can be used for each group of gates rather than each logic gate.

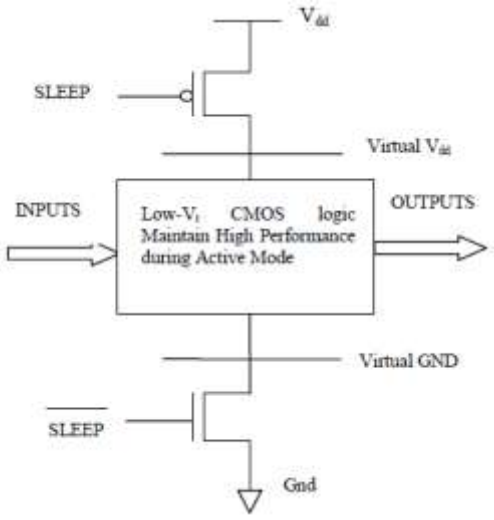

Fig. 4MTMOS Circuit

8. Vector Method:

In this technique, the minimum leakage input vector (MLV) of a circuit is found using the search based algorithm. During standby mode this algorithm is applied to circuit to reduce leakage power. Reduction in leakage current is achieved by modifying the internal logic gates of a circuit. Two Leakage Control Transistors (LCTs-PMOS or NMOS) are placed between the pull up and pull down networks in a specific configuration. Each LCT is driven by the source of the other LCT. This ensures that one of the LCTs is always near cut off region hence reducing the leakage power.[10][12]

9. LECTOR Technique:

This Approach is based in the effective stacking of transistors in the path from supply voltage to ground. The idea behind this method is based on the concept that more than one transistor should be in OFF state in the path from supply to ground because the it causes less leakage than in where only one transistor is OFF in the path from Supply to ground. Two leakage control Transistors (LCTs) were

introduced in each CMOS gate, a PMOS transistor added to the Pull up network and a NMOS transistor to the pull down network. The gate terminal of one LCT is controlled by the source terminal of the other, so that one of the LCTs is in OFF state for any input given to the CMOS gate, by this an additional resistance in the path from supply to ground, decreases sub-threshold leakage current, there by the static power is reduced.[13]

This achieves leakage power reduction without affecting the dynamic power as it does not need any additional circuitry such as for Controlling and Monitoring. It also maintains exact logic state. This Method is used for both Combinational as well as for Memory circuits i.e., SRAM.[14]When this Method is applied to SRAM, the LECTOR technique achieves up to 30-50% savings in leakage power over the Conventional circuit without affecting the dynamic power.[15]

10. Zigzag Method:

This approach reduces wakeup overhead delay caused by the sleep transistors. This is done by placing the alternating sleep transistors based on which the particular network (pull up or pull down) is off for a given specific input vector. The threshold leakage can be reduced by using high threshold voltage sleep transistors. The area of the chip by using this method is slightly increased than by using Sleep transistor Approach.[15]The disadvantage in this method is to estimate the pre scaled vectors for sleep transistors and even the output voltage levels are floating. This floating in the voltage levels can be reduced by reducing the wake-up delay of sleep transistors. This wake up delay is reduced by choosing a particular output state for the circuit and then turning off the pull down circuit for each gate whose output is high, then a pull down sleep transistor is added and if the chosen output is low, and then a pull up sleep transistor is added.[17][18]

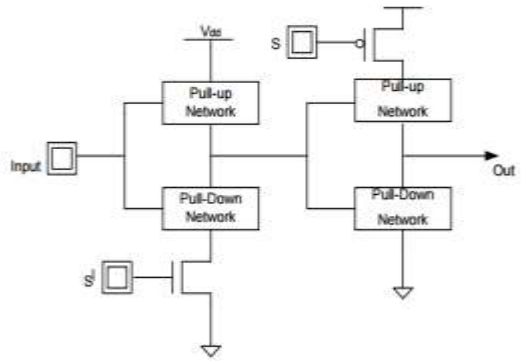

Fig. 5 Zigzag Circuit

III. ANALYSIS

Table 1: Advantages and Disadvantages of different Techniques [14]

Leakage Power Reduction Techniques	Advantages	Disadvantages
Sleep Transistor	Simple Circuitry	Generates noise in circuits
Sleepy Stack	Less delay	Sleep transistors need control circuit
Sleepy Keeper	Less area is required	Decrease in performance
Input Vector Control	High power savings	Control circuit is very complex
Power Gating	Large Power Savings, Best Method	Decreases Voltage Swing
LECTOR	Control circuit is not required, Best power savings in both the modes of operation.	Propagation delay increases because of increased resistance path between source and ground
Forced stacking	Easy to implement, Leakage savings, Easy to fabricate, Single threshold transistors	Propagation delay increases

Table 2: Comparison of leakage reduction techniques [2]

Technique / Parameter	Sleepy Stack	Sleepy keeper	Forced Stack	Sleep transistor
Power (μW)	6.014	5.514	8.782	2.747
Delay (ps)	9	41.5	20	4.5
Current(mA)	0.130	0.100	0.097	.096
Area(μm2)	50.22	50.22	28.50	33.06
Performance	Good	Poor	Good	Poor

Table 3: Percentage of Power Saving, Delay and Area for a S27(ISCAS89 Benchmark) Circuit [14]

Technique	**Power Saving**	**Delay**	**Area**
MTCMOS	10%	4.6-8.4%	2%
VTCMOS	50%	25%	1%
DTCMOS	98%	44%	0

IV. CONCLUSION

In low power VLSI design, leakage power reduction plays a prominent role. As the scaling of technology and in the pursuit of improving the performance of the system, leakage power has increased to a greater extent. Various sub-threshold leakage current reduction techniques have been discussed in this paper and one can opt for a technique depending on the requirement. All the above mentioned techniques are applicable at circuit

level. For more power saving than existing circuit level techniques, leakage reduction techniques can be applied at gate level and block level in the future.

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